

PATENT APPLICATION
Attorney's Docket No. 8750-062
Client Ref. No. SPX200303-0024US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Invéntor(s): Jeong-Hun PARK, et al.

Serial No.: 10/809,076 Examiner: Blum, David S

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Confirmation No.: 7659

Title: SEMICONDUCTOR PROCESS FOR REMOVING DEFECTS DUE TO
EDGE CHIPS OF A SEMICONDUCTOR WAFER AND
SEMICONDUCTOR DEVICE FABRICATED THEREBY

Date: July 19, 2006

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**APPLICANT'S COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR
ALLOWANCE**

In the Examiner's Statement of Reasons for Allowance, the Examiner recited portions of the allowed independent claims and stated that the prior art failed to teach the recited portions. The applications note that it is a well known tenet of patent law that each allowed patent claim stands alone. Further, although the Examiner has indicated at least one reason for allowance, there are other reasons that claims are allowable. In other words, the Examiner has not recited all of the reasons for allowance, and there are reasons for allowability in addition to those given by the Examiner.

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Respectfully submitted,
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